



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/932,228	09/17/1997	KLAUS F. SCHUEGRAF	MICRON.009DV	5093

7590

02/25/2004

Knobbe Martens Olson and Bear
620 Newport Center Drive
Sixteenth Floor
Newport Beach, CA 926608016

EXAMINER

VU, HUNG K

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

08/932,228

Applicant(s)

SCHUEGRAF ET AL.

Examiner

Hung K. Vu

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 December 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-16 and 21-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-16 and 21-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

1. Upon further consideration, the rejection of last Office Action is withdrawn. In view of a further search, however, a new rejection is set forth further below. This rejection is not made final.

Claim Objections

2. Claims 21 and 23 are objected to because of the following informalities:

In claim 21, line 1, “a isolation structures” should be changed to “isolation structures” for clarity

In claim 23, line 2, “dielectric material” should be changed to “halide-doped silicon oxide” for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2811

Claims 11, 14-16 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Venkatesan et al. (PN 5,459,096) in view of Nishiyama et al. (PN 5,429,995, of record). Venkatesan et al. discloses, as shown in Figures 2-8, an isolation structure in a semiconductor substrate comprising,

a recessed portion (38) formed with a vertical sidewall within the semiconductor substrate (30);

a dielectric material (40) filling the recessed portion [Col. 5, lines 27-39].

Venkatesan et al. discloses the dielectric material comprising silicon dioxide. Venkatesan et al. does not disclose the silicon dioxide comprising a halide-dopant. However, Nishiyama et al. discloses an insulating film (22,24,26) for electrically isolation comprises silicon dioxide comprising halide-dopant (fluoride). Note Figures 2A – 11A of Nishiyama et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recessed portion of Venkatesan et al. having the silicon dioxide comprising halide-doped, such as taught by Nishiyama et al. in order to reduce capacitance coupling and to reduce moisture absorption in the insulating film.

With regard to claims 14 and 23, Venkatesan et al. and Nishiyama et al. disclose the isolation structure further comprising a barrier layer disposed between the recessed portion of the semiconductor substrate and the dielectric material.

With regard to claims 15 and 22, Venkatesan et al. and Nishiyama et al. disclose the dielectric material has a dielectric constant lower than 3.9.

With regard to claims 16 and 24, Venkatesan et al. and Nishiyama et al. disclose the dielectric material comprises a fluoride-doped silicon dioxide composition.

With regard to claim 21, Vendatesan et al. discloses, as shown in Figures 2-8, an integrated circuit having a plurality of isolation regions within a semiconductor substrate, each isolation region defined by,

a trench (38) within the semiconductor substrate (30);

a dielectric material (40) filling the trench to form an isolation element [Col. 5, lines 27-39].

Venkatesan et al. discloses the dielectric material comprising silicon dioxide. Venkatesan et al. does not disclose the silicon dioxide comprising a halide-dopant. However, Nishiyama et al. discloses an insulating film (22,24,26) for electrically isolation comprises silicon dioxide comprising halide-dopant (fluoride). Note Figures 2A – 11A of Nishiyama et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recessed portion of Venkatesan et al. having the silicon dioxide comprising halide-doped, such as taught by Nishiyama et al. in order to reduce capacitance coupling and to reduce moisture absorption in the insulating film.

It is noted that the terms “the trench having a characteristic profile produced by an etch process” and “the substrate retaining the characteristic profile of the trench” are method recitations in a device claimed. Note that only the final product is relevant, not the method of making. A product by process claim is directed to the product per se, no matter how actually made. See also

Art Unit: 2811

MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkatesan et al. (PN 5,459,096) in view of Nishiyama et al. (PN 5,429,995, of record) and further in view of Bose et al. (PN 5,492,858, of record).

Venkatesan et al. and Nishiyama et al. disclose the invention substantially as claimed including the isolation structure as recited in the rejection above. Venkatesan et al. and Nishiyama et al. further disclose the recessed portion comprises a trench structure. Venkatesan et al. and Nishiyama et al. do not disclose the trench structure having a ratio of height to width of less than 2:1. However, Bose et al. discloses a trench structure (20,21,22) having a ratio of height to width of less than 2:1. Note Figure 5 of Bose et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench of Venkatesan et al. and Nishiyama et al. having a ratio of height to width of less than 2:1, such as taught by Bose et al. in order to reduce the field threshold voltage and the formation of void in the trench.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Venkatesan et al. (PN 5,459,096) in view of Nishiyama et al. (PN 5,429,995, of record) and further in view of Swan et al. (PN 5,356,838, of record)

Venkatesan et al. and Nishiyama et al. disclose the invention substantially as claimed including the isolation structure as recited in the rejection above. Venkatesan et al. and Nishiyama et al. do not disclose the trench having a depth of less than 200 nm. However, San et al. discloses a

trench having a depth of less than 200 nm. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench of Venkatesan et al. and Nishiyama et al. having a depth of less than 200 nm, such as taught by Swan et al. in order to decrease the void formation and to increase the surface planarity of the final trench structure.

Response to Arguments

6. Applicant's arguments with respect to claims 11 and 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 6:00-3:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The Central Fax Number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

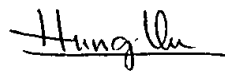
Application/Control Number: 08/932,228

Page 7

Art Unit: 2811

Vu

January 12, 2004

A handwritten signature in black ink, appearing to read "Hung Vu", written over a horizontal line.

Hung Vu

Patent Examiner